
Description: Designing and optimizing large-scale, asynchronous circuits is an iterative process that involves synthesis, simulating, benchmarking, and program rewriting. Throughout the design process, one faces innumerable decisions for program transformation. Intelligent optimization and design-space pruning require detailed knowledge of the run-time behavior of the program. Trace profiling captures typical run-time behavior and input-dependent behavior that cannot be inferred from static analysis alone. This text presents a framework for tracing and analyzing the simulated execution of high-level, concurrent programs, as a foundation for iterative optimization and synthesis of asynchronous circuits. The framework includes an interactive environment and a library of primitive procedures for handling and querying trace data. The extensibility of this framework enables compilation-free development of custom analysis routines. The purpose of this analysis framework is to enable future tools to use profile-driven feedback in automating iterative optimization and design-space exploration.


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