Computer System Design. System-on-Chip

Description: The next generation of computer system designers will be less concerned about details of processors and memories, and more concerned about the elements of a system tailored to particular applications. These designers will have a fundamental knowledge of processors and other elements in the system, but the success of their design will depend on the skills in making system-level tradeoffs that optimize the cost, performance and other attributes to meet application requirements. This book provides a new treatment of computer system design, particularly for System-on-Chip (SOC), which addresses the issues mentioned above. It begins with a global introduction, from the high-level view to the lowest common denominator (the chip itself), then moves on to the three main building blocks of an SOC (processor, memory, and interconnect). Next is an overview of what makes SOC unique (its customization ability and the applications that drive it). The final chapter presents future challenges for system design and SOC possibilities.

Contents:

Preface xiii
List of Abbreviations and Acronyms xvii
1 Introduction to the Systems Approach 1
  1.1 System Architecture: An Overview 1
  1.2 Components of the System: Processors, Memories, and Interconnects 2
  1.3 Hardware and Software: Programmability Versus Performance 5
  1.4 Processor Architectures 7
    1.4.1 Processor: A Functional View 8
    1.4.2 Processor: An Architectural View 9
  1.5 Memory and Addressing 19
    1.5.1 SOC Memory Examples 20
    1.5.2 Addressing: The Architecture of Memory 21
  1.6 System-Level Interconnection 24
    1.6.1 Bus-Based Approach 24
    1.6.2 Network-on-Chip Approach 25
  1.7 An Approach for SOC Design 26
    1.7.1 Requirements and Specifications 26
    1.7.2 Design Iteration 27
  1.8 System Architecture and Complexity 29
  1.9 Product Economics and Implications for SOC 31
    1.9.1 Factors Affecting Product Costs 31
2.10 Problem Set 71

3 Processors 74

3.1 Introduction 74

3.2 Processor Selection for SOC 76

3.2.1 Overview 76

3.2.2 Example: Soft Processors 76

3.2.3 Examples: Processor Core Selection 79

3.3 Basic Concepts in Processor Architecture 81

3.3.1 Instruction Set 81

3.3.2 Some Instruction Set Conventions 82

3.3.3 Branches 82

3.3.4 Interrupts and Exceptions 84

3.4 Basic Concepts in Processor Microarchitecture 86

3.5 Basic Elements in Instruction Handling 88

3.5.1 The Instruction Decoder and Interlocks 88

3.5.2 Bypassing 90

3.5.3 Execution Unit 90

3.6 Buffers: Minimizing Pipeline Delays 91

3.6.1 Mean Request Rate Buffers 91

3.6.2 Buffers Designed for a Fixed or Maximum Request Rate 92

3.7 Branches: Reducing the Cost of Branches 93

3.7.1 Branch Target Capture: Branch Target Buffers (BTBs) 94

3.7.2 Branch Prediction 97

3.8 More Robust Processors: Vector, Very Long Instruction Word (VLIW), and Superscalar 101

3.9 Vector Processors and Vector Instruction Extensions 101

3.9.1 Vector Functional Units 103

3.10 VLIW Processors 107

3.11 Superscalar Processors 108

3.11.1 Data Dependencies 109

3.11.2 Detecting Instruction Concurrency 110

3.11.3 A Simple Implementation 112

3.11.4 Preserving State with Out-of-Order Execution 116
5.8 Layered Architecture and Network Interface Unit 197
5.8.1 NOC Layered Architecture 198
5.8.2 NOC and NIU Example 200
5.8.3 Bus versus NOC 201
5.9 Evaluating Interconnect Networks 201
5.9.1 Static versus Dynamic Networks 202
5.9.2 Comparing Networks: Example 204
5.10 Conclusions 205
5.11 Problem Set 206
6 Customization and Configurability 208
6.1 Introduction 208
6.2 Estimating Effectiveness of Customization 209
6.3 SOC Customization: An Overview 210
6.4 Customizing Instruction Processors 212
6.4.1 Processor Customization Approaches 214
6.4.2 Architecture Description 215
6.4.3 Identifying Custom Instructions Automatically 217
6.5 Reconfigurable Technologies 218
6.5.1 Reconfigurable Functional Units (FUs) 218
6.5.2 Reconfigurable Interconnects 222
6.5.3 Software Configurable Processors 224
6.6 Mapping Designs Onto Reconfigurable Devices 226
6.7 Instance-Specific Design 228
6.8 Customizable Soft Processor: An Example 231
6.9 Reconfiguration 235
6.9.1 Reconfiguration Overhead Analysis 235
6.9.2 Trade-Off Analysis: Reconfigurable Parallelism 237
6.10 Conclusions 242
6.11 Problem Set 243
7 Application Studies 246
7.1 Introduction 246
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.8.1 Visual</td>
<td>296</td>
</tr>
<tr>
<td>8.8.2 Audio</td>
<td>297</td>
</tr>
<tr>
<td>8.9 Motion, Flight, and the Fruit Fly</td>
<td>298</td>
</tr>
<tr>
<td>8.10 Motivation</td>
<td>299</td>
</tr>
<tr>
<td>8.11 Overview</td>
<td>300</td>
</tr>
<tr>
<td>8.12 Pre-Deployment</td>
<td>302</td>
</tr>
<tr>
<td>8.13 Post-Deployment</td>
<td>307</td>
</tr>
<tr>
<td>8.13.1 Situation-Specific Optimization</td>
<td>308</td>
</tr>
<tr>
<td>8.13.2 Autonomous Optimization Control</td>
<td>309</td>
</tr>
<tr>
<td>8.14 Roadmap and Challenges</td>
<td>310</td>
</tr>
<tr>
<td>8.15 Summary</td>
<td>312</td>
</tr>
<tr>
<td>Appendix: Tools for Processor Evaluation</td>
<td>313</td>
</tr>
<tr>
<td>References</td>
<td>316</td>
</tr>
<tr>
<td>Index</td>
<td>329</td>
</tr>
</tbody>
</table>
Fax Order Form

To place an order via fax simply print this form, fill in the information below and fax the completed form to 646-607-1907 (from USA) or +353-1-481-1716 (from Rest of World). If you have any questions please visit http://www.researchandmarkets.com/contact/

Order Information
Please verify that the product information is correct.

Product Name: Computer System Design. System-on-Chip
Web Address: http://www.researchandmarkets.com/reports/2171000/
Office Code: SCAYNBG6

Product Format
Please select the product format and quantity you require:

**Quantity**

| Hard Copy (Hard Back): | USD 108 + USD 28 Shipping/Handling |

* Shipping/Handling is only charged once per order.

Contact Information
Please enter all the information below in BLOCK CAPITALS

<table>
<thead>
<tr>
<th>Title:</th>
<th>Mr</th>
<th>Mrs</th>
<th>Dr</th>
<th>Miss</th>
<th>Ms</th>
<th>Prof</th>
</tr>
</thead>
<tbody>
<tr>
<td>First Name:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Last Name:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Email Address: *</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Job Title:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Organisation:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>City:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Postal / Zip Code:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Country:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Phone Number:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fax Number:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Please refrain from using free email accounts when ordering (e.g. Yahoo, Hotmail, AOL)
Payment Information

Please indicate the payment method you would like to use by selecting the appropriate box.

☐ Pay by credit card: You will receive an email with a link to a secure webpage to enter your credit card details.

☐ Pay by check: Please post the check, accompanied by this form, to:

Research and Markets,
Guinness Center,
Taylors Lane,
Dublin 8,
Ireland.

☐ Pay by wire transfer: Please transfer funds to:

<table>
<thead>
<tr>
<th>Account number</th>
<th>833 130 83</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sort code</td>
<td>98-53-30</td>
</tr>
<tr>
<td>Swift code</td>
<td>ULSBIE2D</td>
</tr>
<tr>
<td>IBAN number</td>
<td>IE78ULSB9853308313083</td>
</tr>
<tr>
<td>Bank Address</td>
<td>Ulster Bank, 27-35 Main Street, Blackrock, Co. Dublin, Ireland.</td>
</tr>
</tbody>
</table>

If you have a Marketing Code please enter it below:

Marketing Code: _______________________

Please note that by ordering from Research and Markets you are agreeing to our Terms and Conditions at http://www.researchandmarkets.com/info/terms.asp