Power Distribution Network Design for VLSI

Description:

The primary goal in VLSI (very large scale integration) power network design is to provide enough power lines across a chip to reduce voltage drops from the power pads to the center of the chip. Voltage drops caused by the power network’s metal lines coupled with transistor switching currents on the chip cause power supply noises that can affect circuit timing and performance, thus providing a constant challenge for designers of high-performance chips. Power Distribution Network Design for VLSI provides detailed information on this critical component of circuit design and physical integration for high-speed chips. A vital tool for professional engineers (especially those involved in the use of commercial tools), as well as graduate students of engineering, the text explains the design issues, guidelines, and CAD tools for the power distribution of the VLSI chip and package, and provides numerous examples for its effective application.

Features of the text include:
- An introduction to power distribution network design
- Design perspectives, such as power network planning, layout specifications, decoupling capacitance insertion, modeling, and analysis
- Electromigration phenomena
- IR drop analysis methodology
- Commands and user interfaces of the VoltageStorm(TM) CAD tool
- Microprocessor design examples using on-chip power distribution
- Flip-chip and package design issues
- Power network measurement techniques from real silicon

The author includes several case studies and a glossary of key words and basic terms to help readers understand and integrate basic concepts in VLSI design and power distribution.

Contents:

Preface.

1 Introduction.

1.1 Power Supply Noise.

1.2 Power Network Modeling.

1.3 Modelling of Switching Currents.

1.4 On-Chip Decoupling Capacitance.

1.5 On-Chip Inductance.

1.6 Process Scaling Impacts.

1.7 Summary.

2 Design Perspectives.

2.1 Planning for Communication Chips.

2.2 Planning for Microprocessor Chips.

2.3 IBM CAD Methodology.

2.4 Design for IR Drop.

2.5 Package-Level Methodology.
2.6 Summary.

3 Electromigration.

3.1 Basic Definitions and EM Rules.

3.2 EM Analysis Tool.

3.3 Full-Chip EM Methodology.

3.4 Summary.

4 IR Voltage Drop.

4.1 Causes of IR Drop.

4.2 Overview of IR Analysis.

4.3 Static Analysis Approach.

4.4 Dynamic Analysis Approach.

4.5 Circuit Analysis with IR Drop Impacts.

4.6 Summary.

5 Power Grid Analysis.

5.1 Introduction.

5.2 Executing the Tool.

5.3 Advanced Static Analysis.

5.4 Dynamic Analysis.

5.5 Layout Exploration.

5.6 Summary.

6 Microprocessor Design Examples.

6.1 Intel IA-32 Pentium-III.

6.2 Sun UltraSPARC.

6.3 Hitachi SuperH Microprocessor.

6.4 IBM S/390 Microprocessor.

6.5 Sun SPARC 64b Microprocessor.

6.6 Intel IA-64 Microprocessor.

6.7 Summary.

7 Package and I/O Design for Power Delivery.

7.1 Flip-Chip Package.

7.2 Simultaneous Switching Noise (SSN).

7.3 Case Study of a Microprocessor-Like Chip.
7.4 Power Supply Measurement.

7.5 I/O Pads for Power/Ground Supplies.

Glossary.

References.

Index.

Ordering: Order Online - http://www.researchandmarkets.com/reports/2173012/

Order by Fax - using the form below

Order by Post - print the order form below and send to

Research and Markets,
Guinness Centre,
Taylors Lane,
Dublin 8,
Ireland.
Fax Order Form
To place an order via fax simply print this form, fill in the information below and fax the completed form to 646-607-1907 (from USA) or +353-1-481-1716 (from Rest of World). If you have any questions please visit http://www.researchandmarkets.com/contact/

Order Information
Please verify that the product information is correct.

Product Name: Power Distribution Network Design for VLSI
Web Address: http://www.researchandmarkets.com/reports/2173012/
Office Code: SCLOPGRX

Product Format
Please select the product format and quantity you require:

Quantity
Hard Copy (Hard Back): USD 111 + USD 28 Shipping/Handling

* Shipping/Handling is only charged once per order.

Contact Information
Please enter all the information below in BLOCK CAPITALS

Title: Mr  Mrs  Dr  Miss  Ms  Prof  
First Name: ___________________________  Last Name: ___________________________
Email Address: * ___________________________
Job Title: ___________________________
Organisation: ___________________________
Address: ___________________________
City: ___________________________
Postal / Zip Code: ___________________________
Country: ___________________________
Phone Number: ___________________________
Fax Number: ___________________________

* Please refrain from using free email accounts when ordering (e.g. Yahoo, Hotmail, AOL)
Payment Information

Please indicate the payment method you would like to use by selecting the appropriate box.

☐ Pay by credit card: You will receive an email with a link to a secure webpage to enter your credit card details.

☐ Pay by check: Please post the check, accompanied by this form, to:
Research and Markets,
Guinness Center,
Taylors Lane,
Dublin 8,
Ireland.

☐ Pay by wire transfer: Please transfer funds to:
Account number 833 130 83
Sort code 98-53-30
Swift code ULSBIE2D
IBAN number IE78ULSB98533083313083
Bank Address Ulster Bank,
27-35 Main Street,
Blackrock,
Co. Dublin,
Ireland.

If you have a Marketing Code please enter it below:

Marketing Code: ______________________________

Please note that by ordering from Research and Markets you are agreeing to our Terms and Conditions at http://www.researchandmarkets.com/info/terms.asp

Please fax this form to:
(646) 607-1907 or (646) 964-6609 - From USA
+353-1-481-1716 or +353-1-653-1571 - From Rest of World