Signal Integrity Effects in Custom IC and ASIC Designs

Description:  "...offers a tutorial guide to IC designers who want to move to the next level of chip design by unlocking the secrets of signal integrity."
—Jake Buurma, Senior Vice President, Worldwide Research & Development, Cadence Design Systems, Inc.
- Covers signal integrity effects in high performance Radio Frequency (RF) IC
- Brings together research papers from the past few years that address the broad range of issues faced by IC designers and CAD managers now and in the future

A Wiley-IEEE Press publication

Contents:
Foreword.

From the Early Days of CMOS to Today.

Signal Integrity: A Problem for Design and CAD Engineers.

Preface.

Acknowledgments.

Signal Integrity Effects in System-on-Chip Designs - A Designer's Perspective.

Part 1: Interconnect Crosstalk.


FastCap: A Multipole Accelerated 3-D Capacitance Extraction Program.

Efficient Coupled Noise Estimation for On-Chip Interconnects.

Switching Window Computation for Static Timing Analysis in Presence of Crosstalk Noise.


Crosstalk Reduction for VLSI.

Noise-aware Repeater Insertion and Wire Sizing For On-Chip Interconnect Hierarchical Moment-Matching.

Post Global Routing Crosstalk Synthesis.

Minimum Crosstalk Channel Routing.

Reducing Cross-Coupling among Interconnect Wires in Deep-Submicron Datapath Design.

A Postprocessing Algorithm for Crosstalk-driven Wire Perturbation.

Noise in Digital Dynamic CMOS Circuits.


Coupling-Driven Signal Encoding Scheme for Low-Power Interface Design.

High Frequency Simulation and Characterization of Advanced Copper Interconnects.

Synthesis of CMOS Domino Circuits for Charge Sharing Alleviation.

Part 2: Inductance Effects.

On-Chip Wiring Design Challenges for Gigahertz Operation.

IC Analyses Including Extracted Inductance Models.

FASTHENRY: A Multipole-Accelerated 3-D Inductance Extraction Program.

Full-Chip, Three-Dimensional, Shapes-Based RLC Extraction.

On-Chip Inductance Modeling and Analysis.

How to Efficiently Capture On-Chip Inductance Effects: Introducing a New Circuit Element K.

Figures of Merit to Characterize the Importance of On-Chip Inductance.

Layout-Techniques for Minimizing On-Chip Interconnect Self Inductance.

A Twisted-Bundle Layout Structure for Minimizing Inductive Coupling Noise.


Full-Chip Verification of UDSM Designs.

Power Supply Noise in Future IC’s: A Crystal Ball Reading.

A Floorplan-based Planning Methodology for Power and Clock Distribution in ASICs.


Full-Chip Signal Interconnect Analysis for Electromigration Reliability.


Simulation and Optimization of the Power Distribution Network in VLSI Circuits.

Design Strategies and Decoupling Techniques for Reducing the Effects of Electrical Interference in Mixed-Mode IC’s.

Design and Analysis of Power Distribution Networks in Power PC Microprocessors.

Modeling the Power and Ground Effects of BGA Packages.


Power Distribution Fidelity of Wirebond Compared to Flip Chip Devices in Grid Array Packages.

Forming Damped LRC Parasitic Circuits in Simultaneously Switched CMOS Output Buffers.

Part 4: Substrate Noise.

Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits.

Principles of Substrate Crosstalk Generation in CMOS Circuits.

Experimental Comparison of Substrate Noise Coupling Using Different Wafer Types.

Modeling and Analysis of Substrate Coupling in Integrated Circuits.
Fast Methods for Extraction and Sparsification of Substrate Coupling.

SUBWAVE: A Methodology for Modeling Digital Substrate Noise Injection in Mixed-Signal ICs.

Substrate Modeling and Lumped Substrate Resistance Extraction for CMOS ESD/Latchup Circuit Simulation.


A Methodology for Measurement and Characterization of Substrate Noise in High Frequency Circuits.


Effects of Substrate Resistances on LNA Performance and a Bondpad Structure for Reducing the Effects in a Silicon Bipolar Technology.

A Study of Oscillator Jitter Due to Supply and Substrate Noise.

CMOS Technology Characterization for Analog and RF Design.

Noise Reduction Is Crucial to Mixed-Signal ASIC Design Success (Parts I & II).

Author Index.

Subject Index.

About the Editor.

Ordering:

Order Online - http://www.researchandmarkets.com/reports/2182440/

Order by Fax - using the form below

Order by Post - print the order form below and send to

Research and Markets,
Guinness Centre,
Taylors Lane,
Dublin 8,
Ireland.
Fax Order Form
To place an order via fax simply print this form, fill in the information below and fax the completed form to 646-607-1907 (from USA) or +353-1-481-1716 (from Rest of World). If you have any questions please visit http://www.researchandmarkets.com/contact/

Order Information
Please verify that the product information is correct.

Product Name: Signal Integrity Effects in Custom IC and ASIC Designs
Web Address: http://www.researchandmarkets.com/reports/2182440/
Office Code: SCAY6PGP

Product Format
Please select the product format and quantity you require:

Quantity
Hard Copy (Hard Back): USD 186 + USD 28 Shipping/Handling

* Shipping/Handling is only charged once per order.

Contact Information
Please enter all the information below in BLOCK CAPITALS

Title: Mr □ Mrs □ Dr □ Miss □ Ms □ Prof □
First Name: ___________________________ Last Name: ___________________________
Email Address: * ___________________________
Job Title: ___________________________
Organisation: ___________________________
Address: ___________________________
City: ___________________________
Postal / Zip Code: ___________________________
Country: ___________________________
Phone Number: ___________________________
Fax Number: ___________________________

* Please refrain from using free email accounts when ordering (e.g. Yahoo, Hotmail, AOL)
Payment Information

Please indicate the payment method you would like to use by selecting the appropriate box.

☐ Pay by credit card: You will receive an email with a link to a secure webpage to enter your credit card details.

☐ Pay by check: Please post the check, accompanied by this form, to:
Research and Markets,
Guinness Center,
Taylors Lane,
Dublin 8,
Ireland.

☐ Pay by wire transfer: Please transfer funds to:

<table>
<thead>
<tr>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Account number</td>
<td>833 130 83</td>
</tr>
<tr>
<td>Sort code</td>
<td>98-53-30</td>
</tr>
<tr>
<td>Swift code</td>
<td>ULSBIE2D</td>
</tr>
<tr>
<td>IBAN number</td>
<td>IE78ULSB98533083313083</td>
</tr>
<tr>
<td>Bank Address</td>
<td>Ulster Bank, 27-35 Main Street, Blackrock, Co. Dublin, Ireland.</td>
</tr>
</tbody>
</table>

If you have a Marketing Code please enter it below:

Marketing Code: ____________________________

Please note that by ordering from Research and Markets you are agreeing to our Terms and Conditions at http://www.researchandmarkets.com/info/terms.asp

Please fax this form to:

(646) 607-1907 or (646) 964-6609 - From USA
+353-1-481-1716 or +353-1-653-1571 - From Rest of World